REMARKS

In the Office Action dated July 12, 2005, the Examiner noted that claims 1-30 are pending in this application, that claims 11 and 25 are objected to as being dependent from a rejected base claim, that the remaining claims are rejected under 35 USC 102 and 35 USC 103, and that the drawings filed on June 22, 2000 are accepted.

In this response, Applicants have presented distinguishing arguments and remarks below.

In view of the above previously filed amendments and the following remarks, Applicants submit that the claims pending in the application are believed to be allowable under 35 U.S.C. §102 and 35 U.S.C. § 103. Thus, Applicants believe that the application is in condition for allowance.

I. REJECTION OF CLAIMS UNDER 35 U.S.C. §102(e)

Claims 1-6, 9, 10, 12-17, 19-22, and 26-30 stand rejected as being anticipated by U.S. Patent 6,067,298 issued to Shinohara. (hereinafter referenced as "Shinohara"). Independent claims 1, 16, and 21 had been previously amended to define Applicants' invention more clearly. Therefore, Applicants respectfully traverse this rejection.

The bases for Applicants' traversal of the rejection are as follows:

- Shinohara stores received ATM cells on a class and output line basis not on an input basis (Claims 1, 16, and 21);
- Shinohara's second "scheduler" does not assign bandwidth (Claims 1 and 21); and
- Shinohara does not adapt the operation of at least one scheduler (Claim 1); and
- Shinohara does not connect his backpressure circuit to the input buffers (Claim 21).

In previously amended claim 1, Applicants call, in part, for "storing received data packets associated with said traffic flows in a respective input buffer wherein each respective input buffer is associated with a particular individual input of the packet switch" and "grouping said traffic flows within a respective input buffer on at least a QoS

guarantee basis". Similarly, in claim 16, Applicants call, in part, for "storing incoming data packets associated with traffic flows in a plurality of input buffers, each buffer in said plurality of input buffers being associated with a particular individual input of the packet switch" and "grouping said traffic flows in each input buffer by QoS classes, each of said QoS classes having a priority level". In apparatus claim 21, Applicants call, in part, for "a first plurality of schedulers for selecting traffic flows arranged in groups based on a particular packet switch input at which the traffic flows are received and at least a QoS guarantee basis".

Claims 1, 16, and 21 call for storage and grouping of the traffic flows on a per-input basis. That is, the traffic flows or data packets received at a particular input are stored and grouped together *"in a respective input buffer wherein each respective input buffer is associated with a particular individual input of the packet switch."* No other traffic flows or data packets from other inputs are stored the respective input buffer. Traffic flows or data packets received from another input are stored in the buffer associated solely with the latter input. In this way, traffic flows or data packets from one input are segregated from the traffic flows or data packets of another input. There is no commingling in a single buffer for traffic flows from one input with traffic flows from other inputs. As a result of this data packet storage, the traffic flow or data packets received at a particular input and stored in the associated buffer are the grouped, as defined in the claims, on at least a Quality of Service basis.

Shinohara shows a plurality of virtual source queues 21 in Figure 1 in input buffer module section 20. These queues are grouped by service class, particularly, by each of the CBR, VBR, ABR, and UBR classes. Within each class, the queues are then organized by output line (output port). The queues 21 are supplied with received (input) ATM cells by class/line separator 25. Class/line separator 25 "identifies the destination output line and the service class type of an ATM cell flowing from the input line 100, and stores it into a proper output line corresponding queue 24. The output line corresponding queue 24 is formed of a virtual source queue 21, a rate control section 22, and a virtual switch internal queue 23." *See Shinohara at col. 6, line 66 et seq.*

Shinohara does not evidence an appreciation for storing ATM cells on the basis of the input from which they were received, as claimed by Applicants. Shinohara does not organize his ATM cells by any scheme or technique even remotely connected to or suggestive of the input port on which the ATM cells were received. Rather, Shinohara's clear intent is to organize the received ATM cells by class and output line. *See Shinohara at col. 2, line 43-47.*

In Shinohara, each queue 21 is only associated with a particular class and a particular output line, not *"with a particular individual input of the packet switch"* as claimed by Applicants. Any one of Shinohara's virtual source queues 21 contains ATM cells from different input ports so long as they are from the same class and are destined for the same output line. The overall queue 24 in which queue 21 resides is even called an "output line corresponding queue of a service class" by Shinohara at col. 12, lines 4-5. It is not a queue for cells from a single associated input.

Shinohara does group the stored packet cells by class. But Shinohara's grouping does not anticipate Applicants' grouping. In Shinohara, the stored cells are organized by output line, not input line. So, when Shinohara groups the stored ATM cells by class, Shinohara obtains a set of service classes that are organized by output line. Shinohara's cells in the same service class from different inputs and destined for the same output line are stored in the same queue. In contrast, Applicants cause cells in the same service class from different inputs destined for the same output line to be stored in the different queues, so that cells in that same service class from the same input destined for the same output line are stored in the same queue.

Nowhere does Shinohara teach, show, or suggest that the traffic flows should be grouped on a per-input basis as defined in claims 1, 16, and 21. Instead, Shinohara clearly shows and teaches the multiplexing of all the inputs together before separating the packets by service class and output line. So by grouping all the input packets together and queuing the commingled packets by service class and output line, not by input line, Shinohara does not even remotely achieve the benefit found by Applicants in keeping packets or traffic flows from the same input together in the same buffer.

Claim 1 calls, in part, for "assigning bandwidth to said selected data packets according to a second plurality of schedulers". Apparatus claim 21 calls for, in part, "a second plurality of schedulers coupled to said first plurality of schedulers for assigning bandwidth to said selected groups of traffic flows". In claims 1 and 21, Applicants make it clear that the second scheduler(s) assigns bandwidth to the data packets.

The Examiner has suggested that Shinohara shows a second scheduler that assigns bandwidth in relation to the 102 rejection. But later, in the 103 rejection on page 11 of the present Office Action, the Examiner states clearly that "the [Shinohara] reference is silent on each of the [second plurality of] schedulers being a Guaranteed Bandwidth Scheduler." This statement should be modified to state that "the Shinohara reference is silent on each of the second plurality of schedulers being a Bandwidth Scheduler", because Shinohara does not have a second scheduler that assigns or guarantees bandwidth. If the interclass priority control section 109 is the second scheduler as suggested by the Examiner, then there is no indication, expressly or impliedly, anywhere in the Shinohara reference that section 109 is even remotely related to bandwidth assignment.

Shinohara's second scheduler does not assign bandwidth to the packets. Shinohara's first scheduler, namely, rate control section 22, sets the transfer rate for packets from queue 21 to queue 23. *See Shinohara, col. 9, lines 21-24, col. 10, lines 47-51, and col. 12, lines 3-9.* No other scheduler in Shinohara sets the rate or bandwidth. The Examiner has identified interclass priority control section 109 as the second scheduler. The operation of section 109 is to multiplex one of the classes output by rotation priority control section 108 onto its output port. *See Shinohara, col. 7, lines 9-15 and col. 10, line 64 to col. 11, line 4.* Clearly, neither section 108 nor section 109 of Shinohara even remotely "assigns bandwidth".

Nowhere does Shinohara teach, show, or suggest that the second scheduler assigns bandwidth to selected data packets as defined in claims 1 and 21. Instead, Shinohara clearly shows and teaches the multiplexing of all the queued packets from different service classes for transmission to the switch fabric.

Claim 1 calls for "adapting the operation of at least one of said first and second schedulers in response to a determination that a utilization level of any output buffer has exceeded a threshold parameter".

Shinohara generates backpressure signals that are supplied to the input modules 20. *See Shinohara, col. 7, line 63 to col. 8, line 5 and col. 8, lines 18-23.* There is no description or figure in Shinohara to show that these signals adapt the operation of at least one of the first and second schedulers as claimed by Applicants. Shinohara does not show the application of these signals to elements 22, 108 or 109. It cannot be inferred that the operation of these elements is adapted in response to the backpressure signals. Instead, Shinohara makes it clear that module 20 alone stops transmitting the packets, not element 22, not element 108, and not element 109. *See Shinohara, col. 11, line 67 to col. 12, line 2.*

Nowhere does Shinohara teach, show, or suggest adapting the operation of at least one of said first and second schedulers in response to a determination that a utilization level of any output buffer has exceeded a threshold parameter as defined in claim 1. Instead, Shinohara clearly shows and teaches that input module 20 responds to the backpressure signals to stop transmission.

In claim 21, Applicants call for "a backpressure-signal circuit connected between each of said respective plurality of output buffers and each of said respective plurality of input buffers, transmitting a stop-transmission signal to each of said respective plurality of input buffers when a threshold parameter in any of said respective plurality of output buffers is exceeded."

Shinohara shows that the backpressure signals are connected to input module 20 but not to the buffers. The Examiner has clearly defined the buffers as element 21. Once this interpretation of the Shinohara reference is made, it cannot be unmade or overlooked when interpreting the reference for other claim limitations. The application of the teachings from the Shinohara reference must be consistent. Since Applicants call for the connective relationship between the input buffers and the backpressure circuit, Shinohara must show that relationship as called for in claim 21 in order to meet that claimed limitation. But Shinohara lacks any showing, teaching or

suggestion of Applicants' claimed connective relationship between the backpressure signals and the input buffers. Thus, Shinohara does not teach this element of Applicants' claim 21.

Since Shinohara does not teach Applicants' claimed storing, grouping, assigning, and adapting steps, Shinohara does not teach, show, or suggest each and every step of the unique method claimed by Applicants in claim 1. Since Shinohara does not teach Applicants' claimed storing and grouping steps, Shinohara does not teach, show, or suggest each and every step of the unique method claimed by Applicants in claim 16. Since Shinohara does not teach Applicants' claimed first plurality of schedulers (storage and grouping), second plurality of schedulers (bandwidth assignment), and backpressure signal circuit, Shinohara does not teach, show, or suggest each and every element of the unique apparatus claimed by Applicants in claim 21. Hence it is believed that Shinohara does not anticipate or make obvious Applicants' claims 1, 16, and 21. Applicants submit that claims 1, 16, and 21 are allowable under 35 U.S.C. §102.

Claims 2-6, 9, 10 and 12-15 depend, either directly or indirectly, from claim 1; claims 17, 19, and 20 are dependent directly from claim 16; and claims 22 and 26-30 depend, either directly or indirectly, from claim 21. Since it has been submitted above that independent claims 1, 16, and 21 are not anticipated by and are not obvious in view of Shinohara, it is further submitted that those claims dependent from claims 1, 16 and 21 are similarly neither anticipated by nor obvious in view of Shinohara. Therefore it is believed that dependent claims 1-6, 9, 10, 12-17, 19-22 and 26-30 are allowable under 35 U.S.C. §102.

In addition to the reasons set forth above, further distinctions are made below for claims 10, 20, and 22. In claims 10, 20, and 22, Applicants call for the following limitations: "each scheduler of said third plurality of schedulers resides in said switch fabric" and "said plurality of output buffers reside in said switch fabric".

In making the rejections of these claims, the Examiner maintains that the core switch 102 and the output buffer 30 of the core switch can be viewed as one unit. But such an interpretation clearly flies in the face of the express teachings of Shinohara. Shinohara clearly states that there are three distinct sections in his apparatus.

Shinohara explains that, "the ATM switching system consists of a core switch section (CS section) 102, an input buffer module section (IXB section) 20, and an output buffer module section (OXB section), 30." *See Shinohara at col. 6, lines 8-11.*

In earlier rejections, the Examiner has said that the third scheduler is Shinohara's element 113, which resides in the output section, not the switch fabric. Shinohara obviously had a choice about where to place the third scheduler and he chose to place it in the output section. Even Shinohara did not suggest combining the output and switch fabric sections. To say otherwise simply ignores and disregards the express teachings of the inventor in the applied reference. It is can only be improper revision and hindsight to ignore such clearly stated words and drawings and then replace them with an inapposite interpretation.

Contrary to the Examiner's interpretation, Shinohara did not place his output buffers in the switch fabric. Shinohara clearly placed the output buffers in the output buffer module section labeled element 30, not 102. Shinohara's express teachings cannot be ignored.

Since Shinohara does not teach Applicants' claimed third schedulers and output buffers in the switch fabric and in light of the reasons set forth earlier in this section with respect to claims 1, 16, and 21, Shinohara does not teach, show, or suggest each and every element of the unique inventions claimed by Applicants in claims 10, 20, and 22. As a result, it is submitted that Shinohara does not anticipate or make obvious Applicants' claims 10, 20, and 22 and that claims 10, 20 and 22 and allowable under 35 U.S.C. §102.

II. REJECTION OF CLAIMS UNDER 35 U.S.C. §103(a)

A. Rejection over Shinohara in view of Regache (Claims 7, 18, & 23)

Claims 7, 18 and 23 stand rejected as being unpatentable over Shinohara in view of U.S. Patent 5,579,312 issued to Regache (hereinafter "Regache"). This rejection is respectfully traversed.

Claim 7 depends from claim 3 and independent claim 1; claim 18 depends from independent claim 16; and claim 23 depends from independent claim 21. Differences

between the independent base claims and the Shinohara reference have been explained immediately above in Section I of this response. Since these dependent claims include all the limitations of their respective independent base claim, each of which is believed to be allowable over Shinohara, the dependent claims are also believed to be allowable over Shinohara alone for the same reasons.

Regache describes a method and apparatus for scheduling transmission of cells of guaranteed bandwidth virtual channels. Regache has been added to the Shinohara reference because the Examiner has stated clearly that "the [Shinohara] reference is silent on each of the [second plurality of] schedulers being a Guaranteed Bandwidth Scheduler."

While Regache does teach guaranteed bandwidth operation of a scheduler, Regache does not teach, show, or suggest that his one and only guaranteed bandwidth scheduler should be used in place of other schedulers, no matter what type. Shinohara shows no apparent need for a guaranteed bandwidth scheduler or a bandwidth scheduler to be used in place of one or more of his schedulers. There is no known motivation from the references themselves to make the combination suggested by the Examiner.

In trying to understand how to effect the suggested combination, it cannot be overlooked that Shinohara has multiple schedulers whereas Regache has only a single scheduler. Should all Shinohara's schedulers be replaced by Regache's scheduler or only the second one because it lacks the bandwidth assignment feature that Applicants claim? If the latter approach for replacement is taken, where is the teaching in either Regache or Shinohara that the second scheduler be replaced with Regache's guaranteed bandwidth scheduler? Bandwidth assignment in the second scheduler is found only in Applicants' specification. But Applicants' specification cannot be used as prior art against itself. So the combination of Regache with Shinohara must be based on impermissible hindsight.

Even if the combination of Regache is made with Shinohara as suggested by the Examiner, the combination would still fail to teach, suggest or show all the limitations in Applicants' claimed invention. The resulting combination would fail to present any

remote suggestion for storing and grouping the traffic flows on a per input basis as described in the remarks above relating to claims 1, 16, and 21. The resulting combination would also lack a suggestion of the adapting step in claim 1. Also, the resulting combination would still fail to meet the connectivity limitation for the backpressure signal circuit in claim 21 as described above. As such, the suggested combination would be completely different from Applicants' claimed method (claims 7 and18) and apparatus (claim 23).

In light of the reasons presented directly above and in Section I of these remarks particularly with respect to independent claims 1, 16, and 21, it is submitted that Applicants' claimed invention would not have been obvious to a person of ordinary skill in the art upon a reading of Shinohara and Regache, separately or in combination, at the time Applicants' invention was made. As a result, claims 7, 18, and 23 are believed to be allowable under 35 U.S.C. §103.

B. Rejection over Shinohara in view of Regache (Claims 8 & 24)

Claims 8 and 24 stand rejected as being unpatentable over Shinohara in view of Regache. This rejection is respectfully traversed.

Claim 8 depends from claim 2 and independent claim 1 and claim 24 depends from independent claim 21. Differences between the independent base claims and the Shinohara reference have been explained immediately above in Section I of this response. Since these dependent claims include all the limitations of their respective independent base claim, each of which is believed to be allowable over Shinohara, the dependent claims are also believed to be allowable over Shinohara alone for the same reasons.

While Regache does teach guaranteed bandwidth operation of a scheduler, Regache does not teach, show, or suggest that his one and only guaranteed bandwidth scheduler should be used in place of other schedulers, no matter what type. Shinohara shows no apparent need for a guaranteed bandwidth scheduler or a bandwidth scheduler in place of his schedulers. There is no known motivation from the references themselves to make the combination suggested by the Examiner.

In trying to understand how to effect the suggested combination, it cannot be overlooked that Shinohara has multiple schedulers whereas Regache has only a single scheduler. Should all of Shinohara's schedulers be replaced by Regache's scheduler or only the third one that lacks the bandwidth assignment feature, which Applicants claim? If the latter approach for replacement is taken, where is the teaching in either Regache or Shinohara that the third scheduler be replaced with Regache's guaranteed bandwidth scheduler? Bandwidth assignment in the third scheduler is found only in Applicants' specification. But Applicants' specification cannot be used as prior art against itself. So the combination of Regache with Shinohara must be based on impermissible hindsight.

Even if the combination of Regache is made with Shinohara as suggested by the Examiner, the combination would still fail to teach, suggest or show all the limitations in Applicants' claimed invention. The resulting combination would fail to present any remote suggestion for storing and grouping the traffic flows on a per input basis as described in the remarks above relating to claims 1 and 21. The resulting combination would also lack a suggestion of the adapting step in claim 1. Also, the resulting combination would still fail to meet the connectivity limitation for the backpressure signal circuit in claim 21 as described above. As such, the suggested combination would be completely different from Applicants' claimed method (claim 8) and apparatus (claim 24).

In light of the reasons presented directly above and in Section I of these remarks particularly with respect to independent claims 1 and 21, it is submitted that Applicants' claimed invention would not have been obvious to a person of ordinary skill in the art upon a reading of Shinohara and Regache, alone or in combination, at the time Applicants' invention was made. As a result, claims 8 and 24 are believed to be allowable under 35 U.S.C. §103.

III. OBJECTION TO CLAIMS & ALLOWABLE SUBJECT MATTER

Objection has been raised to claims 11 and 25 as being dependent from a rejected base claim. It has been noted that these claims would be allowable if rewritten

in independent form including all the limitations of the base claim and any intervening claims.

Applicants thank the Examiner for identifying the allowable subject matter in these claims after considering the previously submitted remarks concerning these claims and the applied art. At this time and in view of the remarks above, Applicants believe that these claims are allowable without further amendment to independent form. Applicants therefore wish to reserve the right to amend these claims at a later time in the prosecution should conditions warrant such action.

CONCLUSION

In view of the foregoing amendments and remarks, Applicants respectfully submit that this application is in condition for allowance. Entry of this amendment, reconsideration and allowance are respectfully solicited.

If, however, the Examiner believes that there are any unresolved issues requiring adverse final action in any of the claims now pending in the application, it is requested that the Examiner telephone Gregory C. Ranieri, Esq. at (732) 280-1390 so that appropriate arrangements can be made for resolving such issues as expeditiously as possible.

Respectfully submitted,

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